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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/730,817	12/08/2003	Daniel Owen	1801270.00134US1	4224

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EXAMINER	
KANG, INSUN	
ART UNIT	PAPER NUMBER
2193	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	04/12/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Notice of this Office communication was sent electronically on the above-indicated "Notification Date" and has a shortened statutory period for reply of 3 MONTHS from 04/12/2007.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/730,817	OWEN ET AL.	
	Examiner	Art Unit	
	Insun Kang	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *2/15/07, /17/06,11/24/06,5/21/04,12/8/03*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,6-18,20,23,25-38,41,43-58 and 80-85* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,6-18,20,23,25-38,41,43-58 and 80-85* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/15/07 and 1/17/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responding to application papers dated 2/15/2007, 1/17/2006, 11/24/2006, 5/21/2004, and 12/8/2003.

2. Claims 1, 4, 6-18, 20, 23, 25-38, 41, 43-58, and 80-85 are pending in the application.

Specification

3. The disclosure is objected to because of the following informalities: in page 2, Figure I needs to be corrected to: Figure 1. In page 1, "0a" in [003] needs to be corrected to "a."

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1, 4, 6-18, 20, 23, 25-38, 41, 43-58, and 80-85 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Per claims 1, 20, and 38, "IR" is interpreted as: "intermediate representation."

Per claim 4, 23, and 41, "base nodes" are interpreted as: "the base nodes."

Per claim 6, 25, and 43, "complex nodes" are interpreted as: "the complex nodes.

Per claim 8, 27, and 45: "complex nodes" are interpreted as: "the complex nodes.

Per claim 10, 29, and 47: "polymorphic nodes" are interpreted as: "the polymorphic nodes.

Per claim 11, 30, and 48: "polymorphic nodes" are interpreted as: "the polymorphic nodes.

Per claim 13, 32, and 50: "polymorphic nodes" is interpreted as: "the polymorphic nodes.

As per claims 9, 12, 14-18, 28, 31, 33-37, 44, 46, 49, 51-58 and 80-85, these claims are objected for dependency on the above objected parent claims 1, 20, and 38.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 4, 7, 8, 14-18, 20, 23, 26, 27, 33-37, 38, 41, 44, 45, 51-55, and 83 are rejected under 35 U.S.C. 102(b) as being anticipated by Souloglou et al. (WO 00/22521, published on 4/2000) hereafter Souloglou.

Per claim 38:

Souloglou discloses:

- a decoding mechanism configured to decode instructions in the subject program code; an intermediate representation generating mechanism configured to generate an

intermediate representation of the decoded instructions (i.e. "translated in Basic Blocks, via an intermediate representation, into code of a target processor," page 2, second paragraph)

- including providing a plurality of possible types of IR nodes in the intermediate representation as abstract representations of the expressions, calculations, and operations performed by the instructions of the subject program code selected from a plurality of possible types of IR nodes including at least base nodes and complex nodes, , and wherein the complex nodes provide a more compact representation of the semantics of complex instructions in the subject program code than that of base node representations (i.e. "*an emulation…to translate …Basic Block by Basic Block*," page 11, lines 21-26; "When a *complex instruction* is decoded from a subject processor code into the intermediate representation," page 13, first paragraph; "*CISC* (Complex Instruction Set Computer) instruction set," page 13, first paragraph (a complex instruction can be decomposed into basic blocks; "if it is determined that no combination is so required, reading directly from the appropriate register," page 5, last 4-5 lines).

-and an intermediate representation type determining mechanism configured to determine which type of IR nodes to generate in the intermediate representation for each respective instruction in the decoded subject program code (i.e. "if there is a stored target code representing a Basic Block for a given entry condition," page 11, second paragraph).

Per claim 41:

Souloglou further discloses:

- wherein base nodes are generic across a plurality of possible subject architectures (i.e. An IR Block is a block of intermediate representation," page 11, third paragraph).

Per claim 44:

Souloglou further discloses:

- wherein a complex node may be decomposed into a plurality of base nodes to represent the same semantics of an instruction in the decoded program code (i.e. "*CISC* (Complex Instruction Set Computer) instruction set," page 13, first paragraph (a complex instruction can be decomposed into basic blocks).

Per claim 45:

Souloglou further discloses:

- wherein the program code is designed to be executed by a subject architecture, the intermediate representation generating mechanism further comprising a complex node generating mechanism for generating complex nodes only for those features correspondingly configurable on the subject architecture (i.e. "if data required for an access lies within more than one valid abstract register," page 6, section c); page 5, last 4-5 lines).

Per claim 51:

Souloglou further discloses:

- wherein the plurality of possible types of IR nodes further include base nodes and architecture specific nodes (i.e. "Basic Blocks...The back End is specific to the target processor," page 16, lines 16-31).

Per claim 52:

Souloglou further discloses:

- wherein the program code is subject code designed for execution on a subject architecture and is dynamically translated into target code for execution on a target architecture (i.e. "The system is a dynamic binary translation system...into target processor code as they are required for execution," page 16, lines 1-3), said intermediate representation generating mechanism further comprising: an architecture specific node generating mechanism for generating the intermediate representation to include architecture specific nodes which are specific to a particular combination of a subject architecture and a target architecture (i.e. "emulation system in response to the form of subject processor...The back End is specific to the target processor," page 11, lines 16-31)

Per claim 53:

Souloglou further discloses:

- initially represent all of the instructions in the subject code as subject architecture-specific nodes, where each subject architecture specific node corresponds to a respective instruction in the subject code (i.e. The system is initialized...the core calls

the front End to decode a first Basic Block of subject processor instructions," page 17, first paragraph)

- determine whether an instruction in the subject code is one in which to provide a target architecture specialized conversion function, convert subject architecture specific nodes into target architecture specific nodes for those instructions determined to provide a target architecture specialized conversion function; and generate base nodes from the remaining subject architecture specific nodes which are not identified as providing a target architecture specialized code generation function (i.e. If during the execution of the translated program, IR Block 2 were to branch back to itself...the state it propagates would be incompatible with the abstract registers states which were originally passed to IR Block 2 by IR Block 1...the intermediate representation is specific to the state of the abstract registers IR Block 2 cannot be re-executed," page 26, last paragraph; "Each IsoBlock is a representation of the same Basic Block of subject processor code, but under different entry conditions," page 27, second paragraph).

Per claim 54:

Souloglou further discloses:

- a specialized target code generating mechanism for generating corresponding target code from the target architecture specific nodes which is specialized for the target architecture (i.e. "The back End is specific to the target processor," page 11, lines 16-31

Per claim 55:

Souloglou further discloses:

- a non specialized target code generating mechanism for generating corresponding target code from the base nodes which is not specialized for the target architecture (i.e. "the core calls the front End to decode a first Basic Block of *subject processor instructions*," page 17, first paragraph).

Per claim 83.

Souloglou further discloses:

Dynamic binary translation from the subject code as binary machine code of a subject instruction set architecture into the target code as binary machine code of a target instruction set architecture (i.e. "The system is a dynamic binary translation system...into target processor code as they are required for execution," page 16, lines 1-3).

Per claims 1, 4, 7, 8, and 14-18, they are the method versions of claims 38, 41, 44, 45, and 51-55, respectively, and are rejected for the same reasons set forth in connection with the rejection of claims 38, 41, 44, 45, and 51-55 above.

Per claims 20, 23, 26, 27, and 33-37, they are the medium versions of claims 38, 41, 44, 45, and 51-55, respectively, and are rejected for the same reasons set forth in connection with the rejection of claims 38, 41, 44, 45, and 51-55 above.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 6, 25, and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Souloglou et al. (WO 00/22521, published 4/2000) hereafter Souloglou in view of Lueh et al. (US Patent 6,292,935) hereafter Lueh.

Per claim 43:

Souloglou does not explicitly teach that complex nodes represent immediate type instructions in which a constant operand value is encoded into the immediate type instruction itself in an immediate field. However, Lueh teaches such nodes was known in the pertinent art, at the time applicant's invention was made, to save a register usage by preserving the operand value within the instruction itself (i.e. immediate operands...which are constant values," col. 5 lines 7-31). It would have been obvious for one having ordinary skill in the art to modify Souloglou's disclosed system to incorporate the teachings of Lueh. The modification would be obvious because one having ordinary skill in the art would be motivated to prevent a register usage as suggested by Lueh (col. 5 lines 7-31).

Per claim 6, it is the method version of claim 43, respectively, and is rejected for the same reasons set forth in connection with the rejection of claim 43 above.

Per claim 25, it is the medium version of claim 43, respectively, and is rejected for the same reasons set forth in connection with the rejection of claim 43 above.

10. Claims 9-13, 28-32, 46-50, 56-58, 80-82, and 84-85 are rejected under 35 U.S.C. 103(a) as being unpatentable over Souloglou et al. (WO 00/22521, published 4/2000) hereafter Souloglou in view of Lattner et al. ("The LLVM Instruction Set and Compilation Strategy," 8/9/2002).

Per claim 46:

Souloglou does not explicitly teach that the plurality of possible types of IR nodes further include polymorphic nodes. However, Lattner teaches such nodes was known in the pertinent art, at the time applicant's invention was made, to perform a single operation on several different types of operands (i.e. "LLVM instructions are polymorphic," a single instruction...can operate on several different types of operands," page 4, section 3.2, third paragraph)." It would have been obvious for one having ordinary skill in the art to modify Souloglou's disclosed system to incorporate the teachings of Lattner. The modification would be obvious because one having ordinary skill in the art would be motivated to reduce the number of distinct opcodes by using polymorphism (page 4, section 3.2, third paragraph) as suggested by Lattner.

Per claim 47.

Souloglou further discloses: wherein the program code is subject code designed for execution on a subject architecture and is dynamically translated into target code for execution on a target architecture, the intermediate representation generating mechanism further comprising (i.e. "The system is a dynamic binary translation system...into target processor code as they are required for execution," page 16, lines 1-3).

Lattner further discloses: a polymorphic node generating mechanism for generating the intermediate representation to include polymorphic nodes, wherein polymorphic nodes contain a function pointer to a function of the target architecture specific to a particular instruction in the subject code (i.e. see section 3.4 Pointer to a function in page 5).

Per claim 48.

Lattner further discloses:

- said polymorphic node generating mechanism generating polymorphic nodes when the features of the target architecture would cause the semantics of a particular subject instruction to be lost if realized as base nodes (i.e. "LLVM instructions are polymorphic...define the semantics of the operation and the type of the result," page 4, section 3.2, third paragraph)."

Per claim 49.

Lattner further discloses:

- wherein each polymorphic node is specific to a combination of a particular instruction in the subject code and a function of the target architecture (i.e. "LLVM instructions are polymorphic," page 4, section 3.2, third paragraph)."

Per claim 50.

Lattner further discloses:

- comprises a polymorphic identification mechanism for identifying an instruction in subject code which corresponds an instruction on a list of polymorphic instructions to be realized as polymorphic nodes (i.e. see section 4.2. The Level Raising Pass in page 11) ; and when a subject instruction corresponds to an instruction on the list of polymorphic instructions, said intermediate representation generating mechanism generates polymorphic nodes only for those subject instructions corresponding to those on the list of polymorphic instructions (i.e. "Most LLVM operations,...are in 3-address form...polymorphic...must follow strict type rules defined," page 4, section 3.2 third paragraph).

Per claim 56.

Lattner further discloses:

- wherein said generated polymorphic nodes specify the registers to be allocated during target code generation (i.e. "LLVM programs transfer values between virtual registers...using typed pointers," page 4, section 3.1).

Per claim 57.

Lattner further discloses:

- wherein said generated polymorphic nodes are utilized in generic kernel optimizations by inferring information from the function pointer in the polymorphic node which may otherwise be indeterminable from the polymorphic node (i.e. "accessed through the pointer values returned by these operations," page 4, section 3.1; see Figure 1 in page 2; 5.3 LLVM Modular Optimizer," page 14, section 5.3; 3.3. Static Single Assignment form, page 4).

Per claim 58:

Lattner further discloses:

- wherein when a subject instruction corresponds to an instruction on the list of polymorphic instructions, said intermediate representation generating mechanism generates either polymorphic nodes or base nodes for those subject instructions corresponding to those on the list of polymorphic instructions (i.e. if control reaches here from basic block label1," page 5. lines 1-22; page 4, section 3.2).

Per claims 9-13 and 80-82, they are the method versions of claims 46-50 and 56-58, respectively, and are rejected for the same reasons set forth in connection with the rejection of claims 46-50 and 56-58 above.

Per claims 28-32 and 84-85, they are the medium versions of claims 46-50 and 56-58, respectively, and are rejected for the same reasons set forth in connection with the rejection of claims 46-50 and 56-58 above.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Insun Kang whose telephone number is 571-272-3724. The examiner can normally be reached on M-R 6:30-5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, MENG Al AN can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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